IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: W. SCHWARZENBACH et al.	Confirmation No.: 9739
Patent No.: 6,987,051 B2	Application No.: 10/733,729
Patent Date: January 17, 2006	Filing Date: December 12, 2003
For: METHOD OF MAKING CAVITIES IN A SEMICONDUCTOR WAFER	Attorney Docket No.: 4717-9200

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 C.F.R. § 1.323

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Patentees hereby respectfully request the issuance of a Certificate of Correction in connection with the above-identified patent. The corrections are listed on the attached Form PTO-1050. The corrections requested are as follows:

Title Page:

Item (75) Inventors, change the city of residence of inventor Maleville from "Terasse" to -- Terrasse --. This change is requested merely to correct a typographical error.

Item (30) Foreign Application Priority Data, change "02 16049" to -- 02 16409 --. Support for this change appears on applicants corrected Declaration filed November 2, 2005. It is further noted that a copy of the correct priority document, French application no. 02 16409, was filed on May 7, 2004 to perfect the priority claim. Furthermore, the filing receipt and the Bibliographic Data sheet on PAIR have been updated to show the correct number.

Column 5:

Line 12, after "duration", delete "AT" and insert -- ΔT --.

Line 14, after "duration", delete "2AT" and insert -- $2\Delta T$ --.

Line 15, after "duration", delete "3AT" and insert -- $3\Delta T$ --.

Line 23, after "durations", delete "AT, 2AT, and 3AT" and insert -- ΔT, $2\Delta T$, and $3\Delta T$ --.

The above changes are to correct errors of a clerical or typographical nature and do not involve changes that would constitute new matter or require reexamination.

A fee of $100 is believed to be due for this request. Please charge the required fees to Winston & Strawn LLP Deposit Account No. 50-1814. Please issue a Certificate of Correction in due course.

Respectfully submitted,

2-6-06

Date

Allan A. Fanucci, Reg. No. 30,256

WINSTON & STRAWN LLP
Customer No. 28765

212-294-3311

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 6,987,051 B2
DATED: January 17, 2006
INVENTORS: Schwarzenbach et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page:
Item (75) Inventors, change the city of residence of inventor Maleville from "Terasse" to -- Terrasse --.
Item (30) Foreign Application Priority Data, change "02 16049" to -- 02 16409 --.

Column 5:
Line 12, after "duration", delete "AT" and insert -- ΔT --.
Line 14, after "duration", delete "2AT" and insert -- $2\Delta T$ --.
Line 15, after "duration", delete "3AT" and insert -- $3\Delta T$ --.
Line 23, after "durations", delete "AT, 2AT, and 3AT" and insert -- ΔT, $2\Delta T$, and $3\Delta T$ --.

WINSTON & STRAWN LLP
Patent Department
1700 K Street, N.W.
Washington, D.C. 20006-3817

US006987051B2

(12) **United States Patent**
Schwarzenbach et al.

(10) **Patent No.: US 6,987,051 B2**
(45) **Date of Patent: Jan. 17, 2006**

(54) **METHOD OF MAKING CAVITIES IN A SEMICONDUCTOR WAFER**

(75) Inventors: **Walter Schwarzenbach**, St. Nazaire les Eymes (FR); **Christophe Maleville**, La Terrasse (FR)

Terrasse — Terasse (FR)

(73) Assignee: **S.O.I.Tec Silicon on Insulator Technologies S.A.**, Bernin (FR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/733,729**

(22) Filed: **Dec. 12, 2003**

(65) **Prior Publication Data**

US 2004/0180519 A1 Sep. 16, 2004

Related U.S. Application Data

(60) Provisional application No. 60/448,124, filed on Feb. 20, 2003.

(30) **Foreign Application Priority Data**

02 16409 Dec. 20, 2002 (FR) 02 16049

(51) **Int. Cl.**
H01L 21/331 (2006.01)

(52) **U.S. Cl.** **438/311**; 438/738

(58) **Field of Classification Search** 438/311, 438/475, 738, 752, 753, 706, 756, 757
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,956,314	A	9/1990	Tam et al.	437/241
5,576,250	A	11/1996	Diem et al.	437/228
5,780,885	A	7/1998	Diem et al.	257/254
5,976,945	A	11/1999	Chi et al.	438/386
6,171,923	B1	1/2001	Chi et al.	438/386
6,246,068	B1 *	6/2001	Sato et al.	257/3
6,294,478	B1 *	9/2001	Sakaguchi et al.	438/753
6,306,729	B1 *	10/2001	Sakaguchi et al.	438/458
6,335,292	B1	1/2002	Li et al.	438/714
6,500,732	B1 *	12/2002	Henley et al.	438/459
6,534,382	B1 *	3/2003	Sakaguchi et al.	438/455
6,569,748	B1 *	5/2003	Sakaguchi et al.	438/455

FOREIGN PATENT DOCUMENTS

FR	2 700 065	7/1994
FR	2 795 554	12/2000
JP	06132262	5/1994

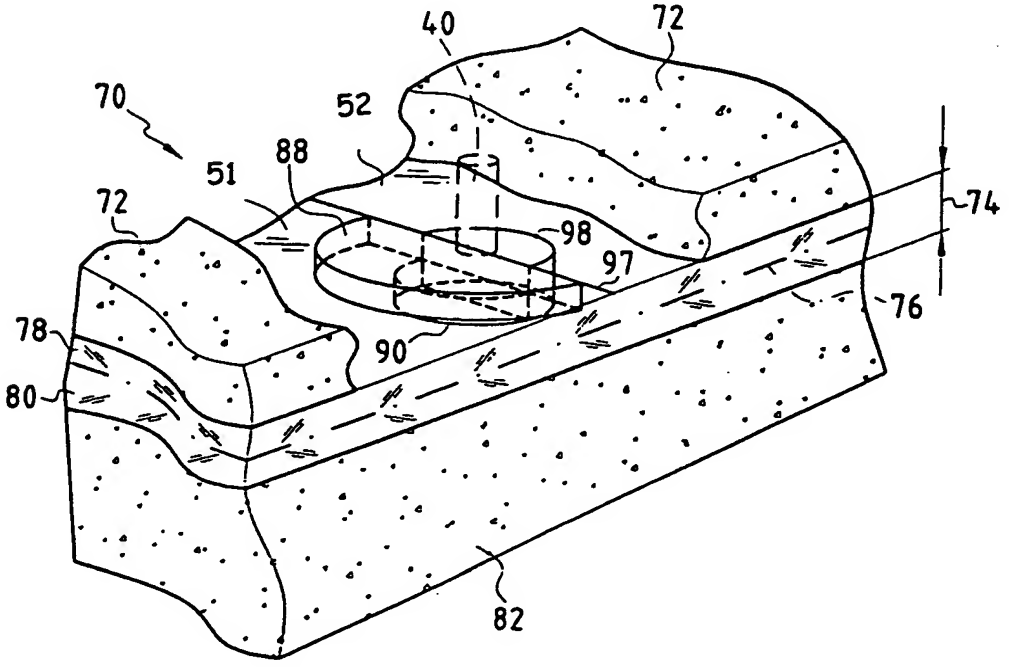
* cited by examiner

Primary Examiner—David Nhu
(74) *Attorney, Agent, or Firm*—Winston & Strawn LLP

(57) **ABSTRACT**

The invention provides a method of making a semiconductor structure that includes a surface layer of silicon, a buried insulating layer, and a substrate. The method includes implanting atoms through at least a portion of the insulating layer; and etching the insulating layer in at least a portion of the layer through which atoms have been implanted.

26 Claims, 3 Drawing Sheets



zone. For example, in FIG. 3A, reference **44** designates the cylinder or etched zone after a duration ΔT, reference **46** designates the etched zone after a duration 2ΔT, and the zone **48** is the zone that has been etched after a duration 3ΔT.

FIG. 3B illustrates hole **53** leading to the buried layer being made at the boundary **57** between the implanted zone **51** and the non-implanted zone **52**, both zones being situated in the insulating layer of silicon dioxide. Etching then takes place simultaneously in both zones **51** and **52**. Etching speeds in the two zones are nevertheless different from each other. That is why the etched zone **54** in the implanted zone **51** is, after duration ΔT, much larger than the corresponding zone **64** in the non-implanted region **52**. Similarly, after a duration 2ΔT the etched region **56** is larger than the etched region **66**, and after a duration 3ΔT the region **58** is larger than the region **68**.

FIG. 3C illustrates hole **62** created in the center of an implanted zone of concave shape **60** situated in the zone **59** that is otherwise not implanted, thus making it possible to create a cavity **69** of square or substantially square shape. In this case, references **65**,**67**, and **69** designate the cavities obtained after respective durations ΔT, 2ΔT, and 3ΔT.

FIG. **4** is a perspective view corresponding to the case shown in FIG. 3B; references **34**, **36**, **38** have the same meanings as in FIG. 2B. The two half-cylinders **58** and **68** pass through the layer of insulation **36** in a direction perpendicular to the plane of said layer and to the plane of the surface layer of silicon **34**. FIG. **4** also illustrates in phantom the hole **40** that is used to direct etchant to the buried insulation layer, with this hole **40** placed on the boundary **57** between the implanted **51** and non-implanted **52** regions. For clarity, a portion of the surface layer has been omitted, it being understood that this portion would remain intact unless etched or otherwise removed.

FIG. **5** shows an SOI structure **70** in which the surface layer of silicon **72** and the insulating or oxide layer **74** have been treated by a flux of ions only to a depth marked by plane **76** (the ion implantation zone or plane). In other words, the insulating or silicon dioxide layer is divided into a top portion **78** through **20** which the flux of ions has passed, and a portion **80** through which the flux of ions has not passed. The speed of etching is then different in these two zones, making it possible to realize etched patterns of section or diameter that varies along an axis perpendicular to the **25** plane **76** or to the plane of the layers **72** and **78**. Reference **82** designates a supporting substrate.

FIG. **6** is a perspective view showing the result of etching the insulating layer **74**. As in FIG. **4**, the hole for directing etchant is illustrated in phantom, with the hole **40** again being placed on the boundary **97** between the implanted **51** and non-implanted **52** portions. Again, part of the surface layer has been omitted for clarity in viewing the remaining portions of the structure.

In the implanted zone **78**, the etched zone **88** is similar to the etched zone **58** in FIG. **4**, however this occurs over a thickness that is smaller than the total thickness of the layer **36**. Etching also takes place in the portion **80**, but at a speed that is slower, thus giving rise to an etched zone **90** situated beneath the zone **88** i.e., at a mean depth that is deeper than the mean depth of the zone **88**. In the plane of the layer **74**, and beyond the boundary **97** between the implanted zone and the non-implanted zone, two portions of insulation situated at two distinct depths have also been etched (each facing a respective etched zone **88** or **90**), however in these zones etching has taken place at the same speed since they are both in a non-implanted region. These zones therefore both have the same diameter or the same dimension and they constitute an etched zone **98**.

It is thus possible to make etched zones situated at depths or at mean depths that are identical or different within the layer of insulation in an SOI structure, these depths being measured from the top of the insulating layer, i.e. where it makes contact with the surface layer **34**, **72** of silicon, or else being measured from the top surface of the surface layer of silicon.

In another aspect, the invention makes it possible to define regions in an insulating layer such as the layer **4** of FIG. **1** in which the speeds of etching in said layer differ from one region to another. The insulating layer then presents at least a first region and a second region having respectively first and second etching speeds that are different from each other.

In an alternative embodiment, the point or location where etching begins may be situated in a zone that is not implanted, with etching subsequently propagating into a zone that has been implanted in which etching takes place at a speed that is different from the speed at which it takes place in the non-implanted zone.

Combining these various techniques mentioned above makes it possible to make etched zones having various sizes in two or three dimensions. Thus, in FIG. **6**, the diameter or largest dimension or characteristic dimension in each portion or etched zone, or the section of said portion or etched zone, varies both in the plane of the layer **74** and in a direction perpendicular to the plane.

It is thus possible to make at least two etched zones in a layer of insulation in an SOI structure, which zones present a first diameter or a first maximum or characteristic dimension, a second diameter or second maximum dimension, different from the first diameter or the first maximum or characteristic dimension, and possibly situated at different depths in the insulating layer.

One and/or both of these zones may be square in section (as in FIG. 3C) or it may be cylindrical (FIG. 3A) or semi-cylindrical (FIG. 3B). Other shapes can also be made, depending on the shape of the mask initially selected for implantation purposes and on the point or location where etching is begun in the implanted region or outside it.

It is also possible to make a cavity of section that is elliptical or polygonal or partially elliptical and partially polygonal in a plane or mean plane parallel to the layer of insulation.

The zone in which atoms are implanted can be of any shape whatsoever, such as convex, concave, or any other shape. This shape of the zone in which atoms are implanted is associated with the final shape desired for the cavity. The shape can be obtained by selection of a mask of similar shape, which mask is applied to the surface of the article prior to implantation. For example, a concave zone can be obtained by the application of a mask that defines a concave open area.

Furthermore, placement of the etchant hole in the center of the shape will assist in minimizing of the etching of adjacent non-implanted areas. Also, a plurality of etchant introduction holes can be made and placed at selected sites within the shape to maximize removal of only the implanted insulation layer in the shape. As a simple example, consider a shape in the form of the number 8; an etchant hole can be placed in each of the top and bottom sections of shape so that etching of the shape is optimized.

Regardless of the invention involved, electronic components such as transistors for example can subsequently be made in the surface layer of silicon **2**, **34**, **72**. The zone